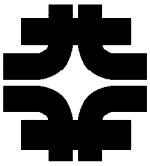

Fermi National Accelerator Laboratory

Engineering Note

M. Utes

Date: 2/9/04

Project: Detector Hybrids
Doc. No: U040209A

Subject: Hybrid Pre-Manufacture Layout Checklist

The following list should be checked prior to sending layout to hybrid manufacturer.

- ☐ 1. General placement of top layers, (Traces, Solder, Bond)
- ☐ 2. Solder Mask Placement
- ☐ 3. Top Layer and Via Layers
- ☐ 4. GNDs on correct pads
- ☐ 5. Power to correct pads
- ☐ 6. No power vias below power layer
- ☐ 7. Via clearance 10 mils
- ☐ 8. GND under all traces
- ☐ 9. Trace to trace spacing (crosstalk)
- ☐ 10. Differential pair spacing vs. adjacent trace spacing
- ☐ 11. Nut Placement
- ☐ 12. Chip placement
- ☐ 13. Connector placement
- ☐ 14. Proper stairstep per layer
- ☐ 15. All vias where necessary
- ☐ 16. Layer 3 via for every layer 7 via
- ☐ 17. No traces connecting to layer 3 vias or layer 7 vias
- ☐ 18. No traces under analog ground
- ☐ 19. Bypassing/decoupling scheme
- ☐ 20. Drill hole placement
- ☐ 21. Silk designators match parts
- ☐ 22. Components connected to correct nets
- ☐ 23. Double-check schematic

Checked by:_____ Date: _____